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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/769,065	01/25/2001	Yoshio Hagihara	15162/03070	7880

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EXAMINER

AGGARWAL, YOGESH K

ART UNIT	PAPER NUMBER
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2615

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/769,065	Applicant(s) HAGIHARA ET AL.	
	Examiner Yogesh K Aggarwal	Art Unit 2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) 1-5 and 10-22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 6-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 January 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>01/25/2001</u> . | 6) <input type="checkbox"/> Other: _____ |

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hynecek et al. (US Patent # 6,323,479) in view of Dierickx (US PG-PUB # 2001/0045508).

[Claim 6]

Hynecek et al. teaches a solid-state image-sensing device (figure 1). Although the figure shows only one pixel, it is inherent that in any application like a camera or a scanner a plurality of pixels are used. The pixel shown is capable of outputting electric signals either in a first mode in which the electric signals are natural-logarithmically proportional to an amount of incident light or in a second mode in which the electric signals are linearly proportional to the amount of incident light (col. 1 lines 10-16, col. 2 lines 52-65, figures 1 and 2). Hynecek et al. fails to specifically disclose a detection circuit for detecting variations in sensitivity among the pixels in each of the first and second modes. However Dierickx disclose a detection circuit (figure 1, elements 2 and 4) for detecting variation in sensitivity among the pixels in logarithmic mode (Paragraphs 25-27, figure 2 disclose a graph showing the pixel output voltage v/s input light intensity. Light sensitivity is defined as light/voltage conversion ratio of a pixel). Therefore taking the combined teachings of Hynecek and Dierickx, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have used a detection circuit as disclosed in Dierickx with the linear-log pixel response of Hynecek in order to remove

Art Unit: 2615

sensitivity variations of the pixels in both modes. The benefit of doing so would be to remove the pixel nonuniformities (sensitivity variations) and to be able to restore the proper value of the photocurrent as taught in Dierickx (Paragraph 27). Although Dierickx does not explicitly talk about the linear response of the pixels, it would be inherently taught in the combination of Hynecek and Dierickx that when the sensor array of Hynecek is used in a linear mode, Dierickx corrects the sensitivity of pixels in linear mode.

[Claim 7]

Dierickx teach a constant-current source (figure 1, element 2) and a switch (figure 1, element 4) for electrically connecting and disconnecting the constant-current source to and from the pixels.

[Claim 8]

Hynecek teach a photoelectric conversion element (figure 1) for outputting an electric signal proportional to an amount of incident light (col. 2 lines 52-53), a first transistor (figure 1, element Q_1) connected in series with the photoelectric conversion element and a second transistor (figure 1, reset transistor), having a control electrode thereof connected to a node between the first transistor and the photoelectric conversion element (col. 2 lines 52-57), for outputting the electric signal, wherein, in the first mode (logarithmic mode), a first voltage is applied to a control electrode (node 1) of the first transistor (Q_1) to make the first transistor operate in a subthreshold region (col. 2 line 66- col. 3 line 13, figure 2, logarithmic response), and wherein, in the second mode (linear mode), the second transistor (reset gate) is used to pre-bias an accumulation node (control node of the first transistor Q_1) to turn the first transistor cut-off (col. 1 lines 10-16).

[Claim 9]

Art Unit: 2615

Dierickx teach a constant-current source (figure 1, element 2) and a switch (figure 1, element 4) for electrically connecting and disconnecting the constant-current source to and from a node between the first transistor (7) and the photoelectric conversion element (1), wherein, when detecting variations in sensitivity among the pixels in the first mode (logarithmic), the first transistor is made to operate in a subthreshold region (Hynecek teaches subthreshold region) and the switch is turned on so that a constant current is fed from the constant-current source through the switch to the first transistor to sample output signals from the pixels (Paragraph 32), and wherein, when detecting variations in sensitivity among the pixels in the second mode (linear), the first transistor cut-off (Hynecek, col. 1 lines 10-16) Although Dierickx does not explicitly talk about the linear response of the pixels, it would be inherently taught in the combination of Hynecek and Dierickx that when the sensor array of Hynecek is used in a linear mode, Dierickx turns the switch on so that a constant voltage is fed through the constant-current source to the control electrode of the second transistor (reset transistor of Hynecek) to initialize the pixels and then sample output signals from the pixels.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.


- i. Collins et al. (US Patent # 6,683,645).
- ii. Dierickx (US Patent # 5,933,190).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K Aggarwal whose telephone number is (703) 305-0346. The examiner can normally be reached on M-F 9:00AM-5:30PM.

Art Unit: 2615

4. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
5. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
December 6, 2004


TUAN HO
PRIMARY EXAMINER